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EXAMINER
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7

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 10/03)

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) FROM
THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed
  after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any
  earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on <u>21 October 2003</u>.

2a)☐ This action is **FINAL**.   2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is
closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) <u>1-26</u> is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) <u>1-26</u> is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on <u>02 December 1999</u> is/are: a)☐ accepted or b)☒ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☐ All b)☐ Some * c)☐ None of:

      1.☐ Certified copies of the priority documents have been received.

      2.☐ Certified copies of the priority documents have been received in Application No. _____.

      3.☐ Copies of the certified copies of the priority documents have been received in this National Stage
      application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application)
since a specific reference was included in the first sentence of the specification or in an Application Data Sheet.
37 CFR 1.78.

    a)☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific
reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1)☒ Notice of References Cited (PTO-892)
2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3)☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .

4)☐ Interview Summary (PTO-413) Paper No(s). _____ .
5)☐ Notice of Informal Patent Application (PTO-152)
6)☐ Other: .

DETAILED ACTION

1.   This action is in response to Pre-Amendment A. This application is filed on 12/02/99.

Claims 1-26 are presented for examination.

Drawings

2.   The drawings are objected to under 37 CFR 1.83(a). The drawings must show every

feature of the invention specified in the claims. Therefore, the "first configurable repetition

period," "PID block," and "ratio block" must be shown or the feature(s) canceled from the

claim(s). No new matter should be entered.

A proposed drawing correction or corrected drawings are required in reply to the Office

action to avoid abandonment of the application. The objection to the drawings will not be held

in abeyance.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-2, 5, 13-14, 17 and 25 are rejected under 35 U.S.C. 103(a) as being

unpatentable over Dailey (US 6,330,483 B1) as applied to claim 1 above, and further in

view of Daggett et al. (hereinafter Daggett) (US 4,786,847).

3.   Referring to claim 1, Dailey teaches a control processor for executing a set of control

tasks defining dynamic model-based interactive control of an industrial process, the control

processor comprising:

- an embedded control task, performed at a relatively low execution priority status within

    the control processor, the embedded control task comprising a multivariable linear

    program including a set of output values corresponding to process setpoints *["channel*

    prioritization in multi-channel control systems", col. 5, lines 27-35, "priorities assigned

    via the Dailey L1 Optimization Algorithm cost function", col. 10, lines 7-17, "lowest

    priority", col. 13, lines 29-42, The present invention can address the relationships

    between primary and secondary controls. It is common for multi-variable control

    systems to designate certain control effectors as primary or secondary", col. 19, lines 46-

    64, see examples of linear algebraic multi-variable matrices with various setpoints in col.

    15, lines 50-65, "linear control system", col. 11, lines 40-44, "linear gain matrices", col.

    2, lines 46-57];

- a set of control blocks, performed at a relatively high execution priority status within the

    control processor, the set of control blocks including regulatory control blocks having

    output values that are transmitted by the control processors to field devices *["higher*

    priority", "prioritization", "important for reasons of safety and system performance

    requirements", "optimal control system", "provides this protection by acting on the

    system's actual state, not just its operator's", col. 14, lines 24-38, "foreground task in

    the embedded control software", col. 37, lines 20-28, "multi-channel aircraft control

    system", col. 2, lines 6-12, "aircraft control system", col. 6, lines 1-7, "invention relates

to control systems, and more particularly to real-time control systems for which an

optimized output is desired", col. 1, lines 1-6, "primary controls", "secondary controls",

"priorities", "allows the plant's full range of achievable control power to be exploited by

a controller", col. 18, lines 22-42].

Dailey does teach both having control blocks having output values that are transmitted by the

control processors to field devices coupled to the industrial process and also having a priority

system *[see above]*. However, the reference of Dailey fails to explicitly teach the connection

between having a high execution priority status and outputting the values from the control

system to the industrial devices. However, Daggett teaches a control system that sets a high

execution priority to the implementation of an industrial device *["SCM implementation, device*

U0096 has the highest priority", col. 39, lines 32-43]. It would have been obvious to one of

ordinary skill in the art at the time the invention was made to have this connection/relationship

between the two to the existing system of Dailey for the reason of maintaining functionality. It is

well known that executing output values of a control system should be at a high priority because

those values are needed for the system or industrial device to work. "Official Notice" is taken

that both the concept and advantages of providing that tasks can be processed from a single

processor is well known and expected in the art. It would have been obvious to one of ordinary

skill in the art at the time the invention was made to include a processor to the existing system

for the reason of having a "brain" such as a control processing unit to control the system.

4.   Referring to claims 2 and 14, Daggett teaches the control processor of claim 1 wherein

the set of control blocks comprise supervisory control blocks *["supervisory control", col. 8,*

lines 30-39, and "supervisory program execution", col. 70, lines 45-47].

5.   Referring to claims 5 and 17, Dailey teaches the method of claims 2 and 14, respectively,

wherein the supervisory control blocks include at least one multivariable loop block, and further

comprising the step of providing an input value for a regulatory control block in accordance with

execution of instructions and data associated with the at least one multivariable loop block *[see*

examples of linear algebraic multi-variable matrices with various setpoints in col. 15, lines 50-

65, "linear control system", col. 11, lines 40-44, "linear gain matrices", col. 2, lines 46-57,

"multi-channel aircraft control system", col. 2, lines 6-12].

6.   Referring to claim 13, Dailey teaches a method for operating a control processor, in an

industrial process control environment, to establish operating values including a set of setpoint

values and a set of process control variables associated with control elements in a controlled

industrial process based upon a set of input variables including process variables provided to the

control processor and representing the present state of the controlled industrial process, the

method comprising the steps of:

-     executing at a lower execution priority, by the control processor, an embedded

        multivariable control application including computer instructions facilitating computing a

        setpoint value corresponding to a process control variable *["channel prioritization in*

        multi-channel control systems", col. 5, lines 27-35, "priorities assigned via the Dailey L1

Optimization Algorithm cost function", col. 10, lines 7-17, "lowest priority", col. 13,

lines 29-4., The present invention can address the relationships between primary and

secondary controls. It is common for multi-variable control systems to designate certain

control effectors as primary or secondary", col. 19, lines 46-64, see examples of linear

algebraic multi-variable matrices with various setpoints in col. 15, lines 50-65, "linear

control system", col. 11, lines 40-44, "linear gain matrices", col. 2, lines 46-57];

-   executing at a higher execution priority, by the control processor, a set of control blocks

    including regulatory control blocks for receiving and storing a set of process variables

    representing the present state of a controlled process *["higher priority", "prioritization",*

    "important for reasons of safety and system performance requirements", "optimal

    control system", "provides this protection by acting on the system's actual state, not just

    its operator's", col. 14, lines 24-38, "multi-channel aircraft control system", col. 2, lines

    6-12, "foreground task in the embedded control software", col. 37, lines 20-28, "aircraft

    control system", col. 6, lines 1-7, "invention relates to control systems, and more

    particularly to real-time control systems for which an optimized output is desired", col.

    1, lines 1-6, "primary controls", "secondary controls", "priorities", "allows the plant's

    full range of achievable control power to be exploited by a controller", col. 18, lines 22-

    42].

Dailey does teach both having control blocks having output values that are transmitted by the

control processors to field devices coupled to the industrial process and also having a priority

system *[see above]*. However, the reference of Dailey fails to explicitly teach the higher

execution priority leading to the present state of a controlled process. However, Daggett teaches

a control system that sets a high execution priority, and when that occurs, an interrupt

brings/resets the system to the current or present state *["SCM implementation, device U0096 has*

the highest priority", "common interrupt request signal", "interrupt", col. 39, lines 32-43]. It

would have been obvious to one of ordinary skill in the art at the time the invention was made to

have an interrupt when a high execution priority has occurred for the reason of maintaining

functionality and improving accuracy of the system. It is well known that interrupts can interrupt

the processing of a control system and redirect the current or present state to somewhere else.

"Official Notice" is taken that both the concept and advantages of providing that tasks can be

processed from a single processor is well known and expected in the art. It would have been

obvious to one of ordinary skill in the art at the time the invention was made to include a

processor to the existing system for the reason of having a "brain" such as a control processing

unit to control the system.

7.   Referring to claim 25, Dailey teaches an industrial process control computer having

multiple operating level including:

-       a background control program execution level wherein the process control computer

        executes an embedded multivariable process control application, the embedded control

        application including instructions for executing a multivariable linear program to

        generate a set of values corresponding to process control variable setpoints *["executed in*

        the background at slower sample period", col. 37, lines 20-28, "channel prioritization in

        multi-channel control systems", col. 5, lines 27-35, see examples of linear algebraic

multi-variable matrices with various setpoints in col. 15, lines 50-65, "linear control

system", col. 11, lines 40-44, "linear gain matrices", col. 2, lines 46-57];

Dailey fails to explicitly teach:

- a foreground control block execution level wherein the process control computer

   executes a set of control blocks, at a higher execution priority level than the background

   control program execution level, the set of control blocks including program instructions

   that, when executed, receive and store a set of process variable values representing the

   state of a controlled process

Dailey does teach a foreground control and that there are priorities of execution levels *["higher*

priority", "prioritization", "important for reasons of safety and system performance

requirements", "optimal control system", "provides this protection by acting on the system's

actual state, not just its operator's", col. 14, lines 24-38, "multi-channel aircraft control

system", col. 2, lines 6-12, "aircraft control system", col. 6, lines 1-7, "invention relates to

control systems, and more particularly to real-time control systems for which an optimized

output is desired", col. 1, lines 1-6, "primary controls", "secondary controls", "priorities",

"allows the plant's full range of achievable control power to be exploited by a controller", col.

18, lines 22-42]. From the reference of Dailey, it is obvious to one of ordinary skill in the art

that the foreground controls of Dailey, executes at a higher execution level than the background

control program because it is common knowledge that the fast, low-latency time signal path

would be desired to be at a higher priority and that is why it is executed on the foreground. And

vice versa, the "slower sample period" would be desired to be at a lower priority and "executed

in the background" [col. 37, lines 20-27].

In addition, Daggett teaches this limitation of foreground controls with respects to high

priority [*"cyclically operated foreground interrupt routine 452 called SERVO", "process*

unscheduled or unexpected interrupts", "highest priority routine 457 called the watch dog timer

interrupt functions in response to operation of the external watch dog hardware", col. 11, lines

40-53]. It would have been obvious to one of ordinary skill in the art at the time the invention

was made to include this feature of high level execution to the foreground control program for

the reason of showcasing the more important aspects of the system. "Official Notice" is taken

that both the concept and advantages of providing that tasks can be processed from a single

processor is well known and expected in the art. It would have been obvious to one of ordinary

skill in the art at the time the invention was made to include a processor to the existing system

for the reason of having a "brain" such as a control processing unit to control the system.

Claims 3-4 and 15-16 are rejected under 35 U.S.C. 103(a) as being unpatentable

over Dailey (US 6,330,483 B1) as applied to claims 9 and 10 above, in view of Daggett et al.

(hereinafter Daggett) (US 4,786,847), and further in view of Morshedi et al. (hereinafter

Morshedi) (US 5,481,716).

8.   Referring to claims 3 and 15, Dailey teaches the control processor of claims 2 and 14,

respectively, wherein the supervisory control blocks include a multivariable control block

including computer instructions facilitating communication or downloading of data between the

control processor and a device. Dailey in view of Daggett fails to explicitly teach the device as

being a workstation. However, Morshedi teaches a control system that uses a workstation

["access", "workstation 300", "database", "data access", col. 4, lines 34-67, see Figure 3]. It

would have been obvious to one of ordinary skill in the art at the time the invention was made to

include workstations to the existing system for the reason of improving the convenience of the

user. With a workstation, a user is able to access to the controls of the process control program

[col. 4, lines 34-47].

9.   Referring to claims 4 and 16, Dailey teaches the control processor of claims 3 and 15,

respectively, wherein the multivariable control block includes computer instructions for

receiving and storing a process control model to be implemented by the embedded control task

["task in the embedded control software", col. 37, lines 20-28, , see examples of linear algebraic

multi-variable matrices with various setpoints in col. 15, lines 50-65, "linear control system",

col. 11, lines 40-44, "linear gain matrices", col. 2, lines 46-57].

Claims 6, 8-12, 20-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over

Dailey (US 6,330,483 B1) as applied to claims 9 and 10 above, in view of Daggett et al.

(hereinafter Daggett) (US 4,786,847), and further in view of McManus et al. (hereinafter

McManus) (US 4,788,647).

10.   Referring to claims 6 and 18, Dailey in view of Draggett fails to explicitly teach the

control processor of claims 5 and 17, respectively, wherein the regulatory control block is a

Proportional-Integral-Derivative (PID) block. However, McManus teaches the regulatory block

being a PID controller *[col. 4, lines 3-11, see Fig 2, item 120]*. It would have been obvious to

one of ordinary skill in the art at the time the invention was made to include a PID control block

to the existing system for the reason of increasing the control of the system by having a feedback

controller such as the PID. It is well known in the art that a PID controller is generally based on

the error between some user defined set point and some measured process variable.

11.   Referring to claim 8, Dailey in view of Daggett fails to explicitly teach the control

processor of claim 1 further comprising a repetition cycle parameter specifying a period for

re-commencing a cycle of the embedded task. However, McManus teaches having a

"SUPERVISOR" that coordinates and controls, such as re-commencing, the execution of other

tasks *["recommence execution until a particular message is received or flag is set", "priority*

scheduling", "SUPERVISOR", coordinating and controlling the execution of other tasks", col.

7, lines 7-56, "configuration parameters for specifying the repetition rate of the task", "number

of a seconds before the first correction, the number of seconds between corrections", col. 16,

lines 8-29]. It would have been obvious to one of ordinary skill in the art at the time the

invention was made to include the feature of supervising the tasks for such controls as re-

commencing for the reason of improving the functionality of the system. As shown in

McManus, a supervisor would have certain controls such as re-commencing for the tasks and is

also used to coordinate tasks with various levels of priority.

12.   Referring to claim 9, McManus teaches the control processor of claim 8 wherein the set

of control blocks includes a supervisory control block including a sequence of instructions to

determine when to re-commence a cycle of the embedded task in accordance with a value

specified by the repetition cycle parameter *["recommence execution until a particular message*

is received or flag is set", "priority scheduling", "SUPERVISOR", coordinating and controlling

the execution of other tasks", col. 7, lines 7-56, "configuration parameters for specifying the

repetition rate of the task", "number of a seconds before the first correction, the number of

seconds between corrections", col. 16, lines 8-29].

13.   Referring to claim 10, Dailey in view of Daggett fails to explicitly teach the control

processor of claim 1 further comprising a block processing cycle parameter specifying a

repetition period for re-commencing a cycle of executing the set of control blocks. However,

McManus teaches having a "SUPERVISOR" that coordinates and controls, such as re-

commencing, the execution of other tasks ["recommence execution until a particular message is

received or flag is set", "priority scheduling", "SUPERVISOR", coordinating and controlling the

execution of other tasks", col. 7, lines 7-56, *"configuration parameters for specifying the*

repetition rate of the task", "number of a seconds before the first correction, the number of

seconds between corrections", col. 16, lines 8-29]. It is well known that a control system has

control blocks. It would have been obvious to one of ordinary skill in the art at the time the

invention was made to include the feature of a block processing cycle parameter specifying a

repetition period for re-commencing an execution cycle for the reason of improving the

functionality and control of the system. As shown in McManus, a supervisor with these

parameter controls would have certain controls such as re-commencing for the tasks and is also used to coordinate tasks with various levels of priority.

14.   Referring to claim 11, McManus teaches the control processor of claim 10 further comprising a repetition cycle parameter specifying a period for re-commencing a cycle of executing the embedded control task tasks *["recommence execution until a particular message is received or flag is set", "priority scheduling", "SUPERVISOR", coordinating and controlling the execution of other tasks", col. 7, lines 7-56, "configuration parameters for specifying the repetition rate of the task", "number of a seconds before the first correction, the number of seconds between corrections", col. 16, lines 8-29].*

15.   Referring to claims 12 and 24, McManus teaches the control processor of claims 11 and 23, respectively, wherein a period specified by the repetition cycle parameter exceeds a period specified by the block processing cycle parameter *["sends a new message to the SUPERVISOR task whenever a full second has expired", col. 11, lines 65-68 through col. 12, lines 1-33].*

16.   Referring to claim 20, Dailey in view of Daggett fails to explicitly teach the method of claim 13 further comprising the step maintaining a repetition cycle parameter specifying a period for re-commencing a cycle of the embedded task. However, McManus teaches having a "SUPERVISOR" that coordinates and controls, such as re-commencing, the execution of other tasks, which include varying the parameters for maintenance *["SUPERVISOR TASK", "configuration parameters, "this step permits these parameters to be temporarily varied during*

plant operation", col. 8, lines 28-50, "recommence execution until a particular message is received or flag is set", "priority scheduling", "SUPERVISOR", coordinating and controlling the execution of other tasks", col. 7, lines 7-56, "configuration parameters for specifying the repetition rate of the task", "number of a seconds before the first correction, the number of seconds between corrections", col. 16, lines 8-29]. It would have been obvious to one of ordinary skill in the art at the time the invention was made to include the feature of maintaining a block processing cycle parameter for re-commencing an execution cycle for the reason of improving the functionality, control and accuracy of the system. As shown in McManus, a supervisor with these parameter controls would have certain controls such as re-commencing for the tasks and is also used to coordinate tasks with various levels of priority. It is well know that varying the parameters will allow for maintenance.

17.   Referring to claim 21, McManus teaches the method of claim 20 wherein the set of control blocks includes a supervisory control block, and further comprising the step of determining, by the supervisory control block, when to re-commence a cycle of the embedded multivariable control application in accordance with a value specified by the repetition cycle parameter *["recommence execution until a particular message is received or flag is set", "priority scheduling", "SUPERVISOR", coordinating and controlling the execution of other tasks", col. 7, lines 7-56, "configuration parameters for specifying the repetition rate of the task", "number of a seconds before the first correction, the number of seconds between corrections", col. 16, lines 8-29].*

18.   Referring to claim 22, Dailey in view of Daggett fails to explicitly teach the method of

claim 13 further comprising the step of maintaining a block processing cycle parameter

specifying a repetition period for re-commencing a cycle of executing the set of control blocks.

However, McManus teaches having a "SUPERVISOR" that coordinates and controls, such as re-

commencing, the execution of other tasks ["recommence execution until a particular message is

received or flag is set", "priority scheduling", "SUPERVISOR", coordinating and controlling the

execution of other tasks", col. 7, lines 7-56, *"configuration parameters for specifying the*

repetition rate of the task", "number of a seconds before the first correction, the number of

seconds between corrections", col. 16, lines 8-29]. It would have been obvious to one of

ordinary skill in the art at the time the invention was made to include the feature of a block

processing cycle parameter specifying a repetition period for re-commencing an execution cycle

for the reason of improving the functionality and control of the system. As shown in McManus,

a supervisor with these parameter controls would have certain controls such as re-commencing

for the tasks and is also used to coordinate tasks with various levels of priority.

19.   Referring to claim 23, it is rejected for the same reasons as stated in the rejection of claim

20.

Claims 7 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over

Dailey (US 6,330,483 B1) as applied to claims 9 and 10 above, in view of Daggett et al.

(hereinafter Daggett) (US 4,786,847), and further in view of Westergren et al. (hereinafter Westergren) (US 5,423,076).

20.   Referring to claims 7 and 19, Dailey and Draggot fails to explicitly teach the control

processor of claims 5 and 17, respectively, wherein the regulatory control block is a ratio block.

Fails to explicitly teach the use of ratio blocks. However, Westergren teaches using ratio blocks

["ratio blocks 146 and 147", col. 9, lines 35-68]. It would have been obvious to one of ordinary

skill in the art at the time the invention was made to include the feature of ratio blocks for the

reason of improving computer capabilities and calculations.

Claim 26 is rejected under 35 U.S.C. 103(a) as being unpatentable by Dailey (US 6,330,483 B1) in view of Wright et al. (hereinafter Wright) (US 6,101,599).

21.   Referring to claim 26, Dailey teaches a multi-level multivariable industrial process

control program execution framework for an industrial control processor including:

-      a first cyclically executed sequence of instructions, repeatedly executed according to a

       first configurable repetition period and at a first level of execution priority, the first

       cyclically executed program executing a sequence of instructions including at least a set

       of instructions for calculating a setpoint value for a process control variable *["channel*

       prioritization in multi-channel control systems", col. 5, lines 27-35, "priorities assigned

       via the Dailey L1 Optimization Algorithm cost function", col. 10, lines 7-17, "lowest

       priority", col. 13, lines 29-42, The present invention can address the relationships

between primary and secondary controls. It is common for multi-variable control

systems to designate certain control effectors as primary or secondary", col. 19, lines 46-

64, see examples of linear algebraic multi-variable matrices with various setpoints in col.

15, lines 50-65, "linear control system", col. 11, lines 40-44, "linear gain matrices", col.

2, lines 46-57];

-   a second cyclically executed sequence of instructions, repeatedly executed according to a

    second repetition period and at a second level of execution priority, the second level of

    priority exceeding the first level of priority, and thus enabling the control processor to

    temporarily suspend execution of the first cyclically executed sequence of instructions in

    order to execute the second cyclically executed sequence of instructions *["higher*

    priority", "prioritization", "important for reasons of safety and system performance

    requirements", "optimal control system", "provides this protection by acting on the

    system's actual state, not just its operator's", col. 14, lines 24-38, "multi-channel

    aircraft control system", col. 2, lines 6-12, "primary controls", "secondary controls",

    "priorities", "allows the plant's full range of achievable control power to be exploited by

    a controller", col. 18, lines 22-42].

It is inherent that the lower priority sequence would be suspended if the higher priority sequence

is executed because that is the purpose of establishing priorities. It is also inherent that the

sequences are cyclic *["begins a new iteration cycle", col. 38, lines 1-3].*

Dailey teaches a first cyclically executed sequence of instructions, repeatedly executed according

to a first configurable repetition period and at a first level of execution priority, the first

cyclically executed program executing a sequence of instructions including at least a set of

instructions for calculating a setpoint value for a process control variable (as shown above) but

fails to explicitly teach that the repetition period can be configurable. However, Wright teaches

a control processor with periods of process cycles that are configurable in order to adjust to

previous process cycles *("configurable minimum number of cycles has elapsed since the*

previous row shifted its phase." Col. 12, lines 10-13). It would have been obvious to one of

ordinary skill in the art at the time the invention was made to include the feature of configurable

repetition periods (cycles) for the reason of increasing the control of the system by being able to

alter or adjust with other cycles in order to properly synchronize. "Official Notice" is taken that

both the concept and advantages of providing that tasks can be processed from a single processor

is well known and expected in the art. It would have been obvious to one of ordinary skill in the

art at the time the invention was made to include a processor to the existing system for the reason

of having a "brain" such as a control processing unit to control the system.

Response to Arguments

22.   *Applicant argues (pg. 10) that Dailey does not teach "first configurable repetition
period."*

Applicant's argument is moot due to the new ground of rejection.

23.   *Applicant argues on page 10 that the Office Action does not identify the presence of
distinct first and second cyclically executed sequences of instructions.*

In response, Examiner respectfully disagrees. It is inherent that a plurality of instructions includes at least 2 different ones. There are two different instructions that handle the differing priority levels.

24.   *Applicant argues on the 4th paragraph of page 11 that nowhere does Dailey suggest that the differing control signal channel priorities are in any way linked to execution priority of code sequences associated with the signal channels.*

In response to applicant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves <u>or in the knowledge generally available to one of ordinary skill in the art</u>. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988)and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992).

25.   *Applicant argues on pages 12 and 14 that Dailey doesn't disclose or suggest the background task executed at a relatively low priority, renders process setpoints.*

In response, Examiner respectfully disagrees. Setpoints make up the components to the multivariable process. Since Dailey teaches a multivariable process, process setpoints are rendered.

26.   *Applicant argues on page 12 that neither Dailey nor the Daggett reference discloses executing the recited embedded task within the control processor that executes control blocks at a relatively high priority to render output values to field devices.*

In response, Applicant does not provide any evidence to this argument. After thorough

consideration, argument is not found to be persuasive. Applicant is directed back to the rejection

of the office action.

27.   *Applicant argues on pages 14-16 that there is no suggestion in either Dailey or Daggett*
that such control blocks can/should be used to carry out the flight control system.

In response to applicant's argument that there is no suggestion to combine the references,

the examiner recognizes that obviousness can only be established by combining or modifying the

teachings of the prior art to produce the claimed invention where there is some teaching,

suggestion, or motivation to do so found either in the references themselves or in the knowledge

generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5

USPQ2d 1596 (Fed. Cir. 1988)and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992).

In this case, it's notoriously well known and obvious that control blocks are components of the

control system which serves to control.

28.   *Applicant argues on page 17 that nowhere does McManus disclose that a supervisory*
control bloack that executes within the control processor.

See paragraph #27. And again, referring to claim 9, McManus teaches the control

processor of claim 8 wherein the set of control blocks includes a supervisory control block

including a sequence of instructions to determine when to re-commence a cycle of the embedded

task in accordance with a value specified by the repetition cycle parameter *["recommence*

execution until a particular message is received or flag is set", "priority scheduling",

"SUPERVISOR", coordinating and controlling the execution of other tasks", col. 7, lines 7-56,

"configuration parameters for specifying the repetition rate of the task", "number of a seconds

before the first correction, the number of seconds between corrections", col. 16, lines 8-29].

Conclusion

Any inquiry concerning this communication or earlier communications from the

examiner should be directed to Kenneth Tang whose telephone number is (703) 305-5334. The

examiner can normally be reached on 8:30AM - 7:00PM, Monday through Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, William Grant can be reached on (703) 308-1108. The fax phone number for the

organization where this application or proceeding is assigned is (703) 746-7239.

Any inquiry of a general nature or relating to the status of this application or proceeding

should be directed to the receptionist whose telephone number is (703) 746-7140.

12/11/03
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